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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
NGO, HUYEN LE	

ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 11/04/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

AK

Office Action Summary	Application No.	Applicant(s)	
	10/817,473	KIM ET AL.	
	Examiner	Art Unit	
	Julie-Huyen L. Ngo	2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *08 September 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-57* is/are pending in the application.

4a) Of the above claim(s) *28, 29 and 34-57* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-27 and 30-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

Applicant's election with traverse of Group I and Species A (claims 1-33; Figs. 1-5) on September 8 2005 is acknowledged.

Applicant's arguments regarding the restriction requirement have been considered; however, the traversal was on the grounds that there is no serious burden on the Examiner in examining all claims 1-57 together. This is not found persuasive since the pixel electrodes of the thin film transistor can be formed with different processes such as directly on substrate or the gate insulating layer or passivation layer.

Further more, claim 28 recites feature: "***the passivation layer comprises a first passivation layer and a second passivation layer, and a plurality of color filters is formed between the first passivation layer and the second passivation layer***", which read on the nonelected species of third embodiment (Figs. 12-13).

Claim 29 recites the feature: "***a plurality of color filters formed over the passivation layer, the plurality of pixel electrodes formed over the plurality of color filters***", which read on the nonelected species of fourth embodiment (Figs. 16-17).

Due to the above reasons, the requirement is deemed proper and is considered to be final.

Accordingly, claims 28, 29 and 34-57 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected inventions and species, there being no allowable generic or linking claim. Claims 1-27, 30-33 read on the elected Species and is treated as follow.

Claim Objections

Claims 22 and 24 are objected to because of the following informalities:

In claim 22, the recitation calling for "the lower films" lacks antecedence. Should claim 22 depend on claim 20?

In claim 24, the recitation calling for "fourth and fifth contact holes" lacks antecedence.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-3 and 5-19, 21, 27 and 30 are rejected under 35 U.S.C. 102(b) as being anticipated by Ikeda (US6172729B1).

With respect to claims 1, 5 and 30, Ikeda teaches (Figs. 1, 2, and 7-8) forming a liquid crystal display comprising the thin film transistor panel, wherein a thin film transistor panel comprising:

- a substrate31;
- a plurality of data lines 11 formed over the substrate and extending in a first direction;

- a plurality of gate lines 12 formed over the substrate and extending in a second direction, the plurality of gate lines crossing the plurality of data lines to form a plurality of pixel areas;
- each of the plurality of pixel areas having a multi-bent band shape as Fig. 1 shown; and a plurality of pixel electrodes each formed in a corresponding pixel area.

wherein

Claim 2:

- each of the plurality of data lines is curved periodically to form the multi-bent band shaped pixel areas.

Claim 3:

- each of the plurality of pixel electrodes comprises a cutout extending in the second direction that divides each of the plurality of pixel electrodes in to a first portion and a second portion.

Claim 5

- the gate lines are also the storage electrode lines

Claim 6:

- the storage electrode lines further comprising:
    - a plurality of sets of storage electrodes 12a connected to each storage electrode line, each set of storage electrodes comprising a pair of first storage electrodes 12a-13 as Fig. 8 shown extending substantially in the

first direction and a second storage electrode that connects the first storage electrodes; and

- a plurality of connectors that connect the first storage electrodes 12-13 in neighboring sets of storage electrodes.

Claim 7:

- each of the first storage electrodes is curved periodically.

Claim 8:

- a gate insulating layer 32 formed over the plurality of gate lines.

Claim 9:

- a plurality of semiconductor stripes33 formed over the gate insulating layer and extending substantially in the first direction.

Claim 10:

- each gate line comprises a plurality of gate electrodes 12 (here gate lines are also gate electrodes).

Claim 11:

- each semiconductor stripe comprises a plurality of projections 33, each projection extending towards a corresponding gate electrode.

Claim 12:

- a plurality of ohmic contact stripes (contact layer 34) and islands formed over the plurality of semiconductor stripes.

Claim 13:

- each ohmic contact stripe comprises a plurality of projections, each of the projections of the contact stripes and the ohmic contact islands located in pairs over the projections of the semiconductor stripes.

Claim 14:

- the plurality of data lines (source electrodes 14a and data lines are the same layer) are formed over the plurality of ohmic contact stripes as shown in Fig. 7.

Claim 15:

- a plurality of drain electrodes each formed over a corresponding ohmic contact island (contact layer 34).

Claim 16:

- each data line comprises a plurality of source electrodes, each source electrode extending towards a corresponding drain electrode so that each source electrode is separated and opposite from a corresponding drain electrode with respect to a corresponding gate electrode.

Claim 17:

- a passivation layer (insulating protective film 36) formed over the plurality of data lines and the plurality of drain electrodes.

Claim 18:

- each data line inherently comprises an expansion portion for electrical connection.

Claim 19:

- each gate line comprises an expansion portion for electrical connection.

Claim 21:

- a gate insulating layer 32 formed over the plurality of gate lines and a passivation layer 36 formed over the plurality of data lines and the plurality of drain electrodes and wherein one of the first storage electrodes in each pair of first storage electrodes has a free end portion and an end portion fixed to a corresponding storage electrode line (also gate lines 12), and another of the first storage electrodes in each pair of first storage electrodes has an end portion that is connected to the connector and an end portion that is fixed to a corresponding storage electrode line.

Claim 27:

- the plurality of semiconductor stripes have substantially the same planar (surface of gate insulating layer 32) as the plurality of data lines and the plurality of drain electrodes

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1-11, 16, 18-19 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Jun (US2004/0201811).

With respect to claims 1 and 30, Jun teaches (Figs. 4&5) forming a liquid crystal display comprising the thin film transistor panel, wherein a thin film transistor panel comprising:

- a substrate 400;
- a plurality of data lines 420 formed over the substrate and extending in a first direction;
- a plurality of gate lines 410 formed over the substrate and extending in a second direction, the plurality of gate lines crossing the plurality of data lines to form a plurality of pixel areas;
- each of the plurality of pixel areas having a multi-bent band shape as Fig. 4 shown; and a plurality of pixel electrodes each formed in a corresponding pixel area.

wherein

Claim 2:

- each of the plurality of data lines is curved periodically to form the multi-bent band shaped pixel areas.

Claim 3:

- each of the plurality of pixel electrodes 440 comprises a cutout extending in the second direction that divides each of the plurality of pixel electrodes 440 in to a first portion and a second portion.

Claim 4:

- each of the plurality of data lines 420 comprise a first set of oblique portions and a second set of oblique portions, the first set of oblique portions being angled counterclockwise by about 45 degrees from the plurality of gate lines and the

second set of oblique portions being angled clockwise by about 45 degrees from the plurality of gate lines.

Claim 5:

- a plurality of storage electrode lines 480 formed over the substrate and extending substantially in the second direction.

Claim 6:

- the storage electrode lines further comprising:
    - a plurality of sets of storage electrodes 480 connected to each storage electrode line, each set of storage electrodes comprising a pair of first storage electrodes 470 Fig. 4 shown extending substantially in the first direction and a second storage electrode that connects the first storage electrodes; and
    - a plurality of connectors that connect the first storage electrodes in neighboring sets of storage electrodes.

Claim 7:

- each of the first storage electrodes 470 is curved periodically.

Claim 8:

- a gate-insulating layer inherently formed over the plurality of gate lines.

Claim 9:

- a plurality of semiconductor stripes inherently formed over the gate insulating layer and extending substantially in the first direction.

Claim 10:

- each gate line comprises a plurality of gate electrodes 432.

Claim 11:

- each semiconductor stripe comprises a plurality of projections, each projection extending towards a corresponding gate electrode to form U-shape TFT.

Claim 16:

- each data line comprises a plurality of source electrodes 434, each source electrode extending towards a corresponding drain electrode 436 so that each source electrode is separated and opposite from a corresponding drain electrode with respect to a corresponding gate electrode.

Claim 18:

- each data line inherently comprises an expansion portion for electrical connection.

Claim 19:

- each gate line inherently comprises an expansion portion for electrical connection.

Claims 1-3 and 5-19, 21 and 30 are rejected under 35 U.S.C. 102(e) as being anticipated by Lee (US6710836B2).

With respect to claims 1 and 30, Jun teaches (Figs. 5-6 and 9) forming a liquid crystal display comprising the thin film transistor panel, wherein a thin film transistor panel comprising:

- a substrate 110;

- a plurality of data lines 161 formed over the substrate and extending in a first direction;
- a plurality of gate lines 121 formed over the substrate and extending in a second direction, the plurality of gate lines crossing the plurality of data lines to form a plurality of pixel areas;
- each of the plurality of pixel areas having a multi-bent band shape as Fig. 5 shown; and a plurality of pixel electrodes each formed in a corresponding pixel area.

wherein

Claim 2:

- each of the plurality of data lines is curved periodically to form the multi-bent band shaped pixel areas.

Claim 3:

- each of the plurality of pixel electrodes 192 comprises a cutout extending in the second direction that divides each of the plurality of pixel electrodes in to a first portion and a second portion as shown in fig. 5.

Claim 5:

- a plurality of storage electrode lines 181 formed over the substrate and extending substantially in the second direction.

Claim 6:

- the storage electrode lines 181 further comprising:

- a plurality of sets of storage electrodes 181 connected to each storage electrode line, each set of storage electrodes (common electrodes) comprising a pair of first storage electrodes 184 (as shown in Fig. 5) extending substantially in the first direction and a second storage electrode 165 that connects the first storage electrodes; and
- a plurality of connectors that connect the first storage electrodes in neighboring sets of storage electrodes.

Claim 7:

- each of the first storage electrodes 184 is curved periodically.

Claim 8:

- a gate insulating layer 130 formed over the plurality of gate lines.

Claim 9:

- a plurality of semiconductor stripes 141 formed over the gate insulating layer and extending substantially in the first direction.

Claim 10:

- each gate line comprises a plurality of gate electrodes 122.

Claim 11:

- each semiconductor stripe comprises a plurality of projections, each projection extending towards a corresponding gate electrode.

Claim 12:

- a plurality of ohmic contact stripes 151-152 and islands formed over the plurality of semiconductor stripes.

Claim 13:

- each ohmic contact stripe comprises a plurality of projections, each of the projections of the contact stripes and the ohmic contact islands located in pairs over the projections of the semiconductor stripes.

Claim 14:

- the plurality of data lines (source electrodes 162 and data lines 161 are the same layer) are formed over the plurality of ohmic contact stripes 151 as shown in Figs. 5&6.

Claim 15:

- a plurality of drain electrodes 163 each formed over a corresponding ohmic contact island 152.

Claim 16:

- each data line 161 comprises a plurality of source electrodes 162, each source electrode162 extending towards a corresponding drain electrode 163 so that each source electrode is separated and opposite from a corresponding drain electrode with respect to a corresponding gate electrode.

Claim 17:

- a passivation layer 170 formed over the plurality of data lines and the plurality of drain electrodes.

Claim 18:

- each data line inherently comprises an expansion portion for electrical connection.

Claim 19:

- each gate line inherently comprises an expansion portion for electrical connection.

Claim 21:

- a gate insulating layer 130 formed over the plurality of gate lines 121and a passivation layer 170 formed over the plurality of data lines 161 and the plurality of drain electrodes 163 and wherein one of the first storage electrodes in each pair of first storage electrodes has a free end portion and an end portion fixed to a corresponding storage electrode line, and another of the first storage electrodes in each pair of first storage electrodes has an end portion that is connected to the connector and an end portion that is fixed to a corresponding storage electrode line.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 20 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US6172729B1) as applied above to claims 1-3 and 5-19, and further in view of Chae (US6861368B2).

Ikeda fails to disclose the features in claims 20 and 22-25.

Chae teaches (Figs. 4-5) forming a thin film transistor panel comprising the plurality of data lines 174 and plurality of drain electrodes 178, each comprises a lower film (barrier layer 174) and upper film (copper layer); wherein

- the passivation layer comprises a plurality of first contact holes at 180 exposing the lower films of the plurality of drain electrodes and a plurality of second contact holes at 184 exposing the lower films of the expansions of the plurality of data lines, and a plurality of third contact holes at 182 exposing the expansions of the plurality of gate lines for improving electric characteristic due to an inferior contact property without organic residue from passivation layer;
- fourth and fifth contact holes have not been identified; thereby examiner may consider them as one of first, second, and third contact holes.
- the plurality of pixel electrode is formed over the passivation layer and is electrically connected to the plurality of drain electrodes through the first contact holes for improving display aperture.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a thin film transistor panel disclosed by Ikeda with a plurality of data lines and plurality of drain electrodes, each comprises a lower film (barrier layer 174) and upper film (copper layer);

wherein

(a) the passivation layer comprises a plurality of first contact holes exposing the lower films of the plurality of drain electrodes and a plurality of second contact holes

exposing the lower films of the expansions of the plurality of data lines, and a plurality of third contact holes exposing the expansions of the plurality of gate lines for improving electric characteristic due to an inferior contact property without organic residue from passivation layer (col. 3 lines 37-38), as taught by Chae;

(b) the plurality of pixel electrode are formed over the passivation layer and are electrically connected to the plurality of drain electrodes through the first contact holes for improving display aperture (col. 3 lines 44-46), as taught by Chae.

Claims 20 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jun (US2004/0201811) as applied above to claims 1-11, 16 and 18-19 and further in view of Chae (US6861368B2).

Jun fails to disclose the features recited in claims 20 and 22-25.

Chae teaches (Figs. 4-5) forming a thin film transistor panel comprising the plurality of data lines 174 and plurality of drain electrodes 178, each comprises a lower film (barrier layer 174) and upper film (copper layer); wherein

- the passivation layer comprises a plurality of first contact holes at 180 exposing the lower films of the plurality of drain electrodes and a plurality of second contact holes at 184 exposing the lower films of the expansions of the plurality of data lines, and a plurality of third contact holes at 182 exposing the expansions of the plurality of gate lines for improving electric characteristic due to an inferior contact property without organic residue from passivation layer;

- fourth and fifth contact holes have not been identified; thereby examiner may consider them as one of first, second, and third contact holes.
- the plurality of pixel electrode are formed over the passivation layer and are electrically connected to the plurality of drain electrodes through the first contact holes for improving display aperture.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a thin film transistor panel disclosed by Jun with a plurality of data lines and plurality of drain electrodes, each comprises a lower film (barrier layer 174) and upper film (copper layer); wherein (a) the passivation layer comprises a plurality of first contact holes exposing the lower films of the plurality of drain electrodes and a plurality of second contact holes exposing the lower films of the expansions of the plurality of data lines, and a plurality of third contact holes exposing the expansions of the plurality of gate lines for improving electric characteristic due to an inferior contact property without organic residue from passivation layer (col. 3 lines 37-38); (b) the plurality of pixel electrode are formed over the passivation layer and are electrically connected to the plurality of drain electrodes through the first contact holes for improving display aperture (col. 3 lines 44-46), as taught by Chae.

Claims 20 and 22-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US6710836B2) as applied above to claims 1-3 and 5-19 and 21 and further in view of Chae (US6861368B2).

Lee fails to disclose the features recited in claims 20 and 22-25.

Chae teaches (Figs. 4-5 and col. 3 lines 44-46) forming a thin film transistor panel comprising the plurality of data lines 174 and plurality of drain electrodes 178, each comprises a lower film (barrier layer 174) and upper film (copper layer); wherein

- the passivation layer comprises a plurality of first contact holes at 180 exposing the lower films of the plurality of drain electrodes and a plurality of second contact holes at 184 exposing the lower films of the expansions of the plurality of data lines, and a plurality of third contact holes at 182 exposing the expansions of the plurality of gate lines for improving electric characteristic due to an inferior contact property without organic residue from passivation layer;
- fourth and fifth contact holes have not been identified; thereby examiner may consider them as one of first, second, and third contact holes.
- the plurality of pixel electrode are formed over the passivation layer and are electrically connected to the plurality of drain electrodes through the first contact holes for improving display aperture.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a thin film transistor panel disclosed by Lee with a plurality of data lines and plurality of drain electrodes, each comprises a lower film (barrier layer 174) and upper film (copper layer); wherein (a) the passivation layer comprises a plurality of first contact holes exposing the lower films of the plurality of drain electrodes and a plurality of second contact holes exposing the lower films of

the expansions of the plurality of data lines, and a plurality of third contact holes exposing the expansions of the plurality of gate lines for improving electric characteristic due to an inferior contact property without organic residue from passivation layer (col. 3 lines 37-38); (b) the plurality of pixel electrode are formed over the passivation layer and are electrically connected to the plurality of drain electrodes through the first contact holes for improving display aperture, as taught by Chae.

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US6172729B1) as applied above to claims 1-3 and 5-19, 21, and further in view of Um et al. (US20030133055A1).

Ikeda fails to disclose the feature recited in claim 26.

Um et al. teach (Figs. 1 and 9) forming a thin film transistor panel, wherein the passivation layer 180 and the gate insulating layer 140 comprise a plurality of fourth contact holes 185 (see fig. 1) exposing portions of the storage electrode lines proximate the fixed end of a corresponding storage electrode having a free end and a plurality of fifth contact holes 184 (see fig. 1) exposing free end portions of the storage electrodes having a free end and a plurality of storage connecting bridges 91 (see fig. 1) formed over the passivation layer that cross over the plurality of gate lines and electrically connect neighboring storage electrode lines through the plurality of fourth contact holes and the plurality of fifth contact holes for enhancing electrical connections between the gate lines and the storage bridges when irradiating a laser beam for such repair, as taught by Um et al. (paragraph 96 lines 14-16).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a thin film transistor panel disclosed by Ikeda with the passivation layer and the gate insulating layer comprising a plurality of fourth contact holes exposing portions of the storage electrode lines proximate the fixed end of a corresponding storage electrode having a free end and a plurality of fifth contact holes exposing free end portions of the storage electrodes having a free end and a plurality of storage connecting bridges formed over the passivation layer that cross over the plurality of gate lines and electrically connect neighboring storage electrode lines through the plurality of fourth contact holes and the plurality of fifth contact holes for enhancing electrical connections between the gate lines and the storage bridges when irradiating a laser beam for such repair, as taught by Um et al. (paragraph 96 lines 14-16).

Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Lee (US6710836B2) as applied above to claims 1-3, 5-19, and 21, and further in view of Um et al. (US20030133055A1).

Lee fails to disclose the feature recited in claim 26.

Um et al. teach (Figs. 1 and 9) forming a thin film transistor panel having the passivation layer 180 and the gate insulating layer 140 comprising a plurality of fourth contact holes 185 (see Fig. 1) exposing portions of the storage electrode lines proximate the fixed end of a corresponding storage electrode having a free end and a plurality of fifth contact holes 184 (see Fig. 1) exposing free end portions of the storage electrodes having a free end and a plurality of storage connecting bridges 91(see Fig. 1)

formed over the passivation layer that cross over the plurality of gate lines and electrically connect neighboring storage electrode lines through the plurality of fourth contact holes and the plurality of fifth contact holes for enhancing electrical connections between the gate lines and the storage bridges when irradiating a laser beam for such repair, as taught by Um et al. (paragraph 96, lines 14-16).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify Lee thin film transistor panel with a passivation layer and the gate insulating layer comprise a plurality of fourth contact holes exposing portions of the storage electrode lines proximate the fixed end of a corresponding storage electrode having a free end and a plurality of fifth contact holes exposing free end portions of the storage electrodes having a free end and a plurality of storage connecting bridges 91 formed over the passivation layer that cross over the plurality of gate lines and electrically connect neighboring storage electrode lines through the plurality of fourth contact holes and the plurality of fifth contact holes for enhancing electrical connections between the gate lines and the storage bridges when irradiating a laser beam for such repair as taught by Um et al. (paragraph 96 lines 14-16).

Claim 31-33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ikeda (US6172729B1) in view of Tusujimura et al. (US 5626796 A).

With respect to claim 31, Ikeda teaches (Figs. 1, 2, and 7-8) forming a liquid crystal display comprising:

- a thin film transistor panel comprising:
    - a first substrate 31;
    - a plurality of data lines 11 formed over the first substrate and extending in a first direction;
    - a plurality of gate lines 12 formed over the first substrate and extending in a second direction, the plurality of gate lines crossing the plurality of data lines to form a plurality of pixel areas, each of the plurality of pixel areas having a multi-bent band shape; and
    - a plurality of pixel electrodes 13 each formed in a corresponding pixel area;
- a common electrode panel (col. 5, lines 49-66) comprising:
    - a second substrate (opposed substrate);
    - colors formed over the second substrate; and
    - a common electrode (opposed electrode) formed over the second substrate;
- a liquid crystal layer (col. 5, lines 53-55) formed between the thin film transistor panel and the common electrode panel.

wherein

Claim 32:

- each of the plurality of pixel electrodes comprises a cutout extending in the second direction that divides each of the plurality of pixel electrodes in to a first portion and a second portion as shown in Fig. 1.

However, Ikeda fails to teach a common electrode panel comprising the black matrix formed over the second substrate and a plurality of color filters formed over the black matrix and the second substrate.

Tusujimura et al. teach (Fig. 1 and col. 1 lines 17-22) forming a common electrode panel comprising the black matrix 24 formed over the second substrate and a plurality of color filters 32 formed over the black matrix and the second substrate 30 for improving the contrast ratio of displayed images to the background.

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify Ikeda liquid crystal display with a common electrode panel comprising the black matrix 24 formed over the second substrate and a plurality of color filters 32 formed over the black matrix and the second substrate 30 for improving the contrast ratio of displayed images to the background, as taught by Tusujimura et al.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

Song et al. (US 6900871 B1) disclose a thin film transistor substrate that increases an aperture ratio as well as prevents shorts between pixel electrodes by connecting drain electrodes of thin film transistors to storage electrodes to reduce the number of holes contacting the pixel electrodes.

Ochiai et al. (6897909 B2) disclose a liquid crystal display device, a capacitance element uses a semiconductor layer as one electrode and is formed between the semiconductor layer and a storage capacitance line with an insulating film interposed therebetween, and a voltage which constantly brings a MOS type transistor into an ON state is applied to the storage capacitance line.

Okada et al. (US 6633360) disclose an active matrix type liquid crystal display apparatus, each of pixel electrodes has overhanging portions at its opposite side edges. These overhanging portions of the pixel electrode cover two signal lines placed on opposite sides of the pixel electrode, respectively.

Contact Information

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Julie-Huyen L. Ngo whose telephone number is (571) 272-2295. The Examiner can normally be reached on T-Friday.

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's Supervisor, Mr. Robert H. Kim can be reached at (571) 272-2293.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (571) 272-1562.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

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Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

November 2, 2005

Julie -Huyen L. Ngo
Primary Patent Examiner
Art Unit 2871